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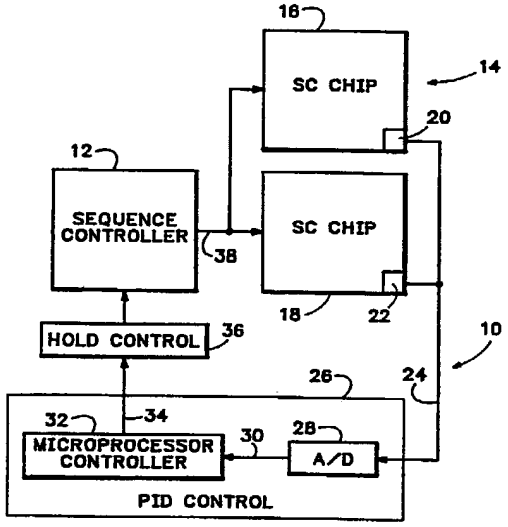

(57) Abstract

A temperature-control system includes an integrated circuit (14) and a sequence controller (12) therefore, wherein the sequence controller (12) provides instructions and/or data to the integrated circuit (14) which performs operations according to the instructions on the data. A temperature recognition intervention mechanism is provided which intervenes, via the sequence controller (12), with the operational rate of the integrated circuit (14) in relation to different temperature conditions which occur in the integrated circuit (14), thus providing security against temperature-induced damage to the integrated circuit (14). A method of the invention includes detecting a temperature-related parameter of the integrated circuit (14), determining the rate of change of the temperature (76) of the integrated circuit (14) and, if the rate of change indicates that the integrated circuit (14) will exceed a first predetermined temperature, providing noop (82) instructions to the integrated circuit (14) for a predetermined number of system cycles to allow the integrated circuit (14) to cool to an acceptable temperature. If the rate of change of the temperature indicates that the integrated circuit (14) will reach a temperature higher than a second predetermined temperature value, the frequency of noop instructions will increase or the integrated circuit (14) will be shut down (86).

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TEMPERATURE-SENSING CONTROL SYSTEM AND METHOD FOR INTEGRATED CIRCUITS

Technical Field

The invention relates to a computer processor architecture for preventing heat damage to integrated circuits, and specifically to a temperature-sensing control system and method for use with integrated circuits.

Background Art

Integrated circuits provide a great deal of electronic circuitry in a very small space. As the size and processor density of integrated circuits, sometimes referred to as computer chips, increases, the heat which is generated during circuit operation is not readily dissipated. This produces higher operating temperatures, and in some instance, can result in the failure of the circuitry contained in the chip due to excessive heat. Even if the circuit is not destroyed, the circuit will operate less efficiently as the resistance of any electrical component generally increases as the temperature of the component increases.

For most integrated circuits, excessive heat buildup is not a significant problem, and the heat which is buildup may be carried off by attaching the chip to a heat sink, which will dissipate heat.

Certain types of integrated circuits, such as highly parallel integrated circuits, like neural network circuits used for pattern classification or recognition, tend to operate in a "bursty" fashion, wherein the circuit may remain idle for a period of time and then operate at its maximum, or close to its maximum, capacity for a period of time. During periods of time when the circuit is operating at or near maximum capacity, the temperature of the chip may raise as maximum power is drawn by the circuit. Any integrated circuit which is operated in a limited power environment may suffer from temperature increases that may potentially damage the circuit.

Because it is impractical to design an integrated circuit to dissipate maximum power when maximum power is not constantly applied to the circuit, it is conceivable that the maximum operating temperature of the circuit will be exceeded during maximum power operations, thereby damaging or destroying the circuit. If, for instance, the maximum power that an

integrated circuit draws is 5 watts, and the nominal operating power is in the vicinity of 2 watts, the integrated circuit will be designed to readily dissipate the heat generated when the circuit is operating at 2 watts. Because of thermal inertia in the integrated circuit, the heat buildup and dissipation will lag behind the median or high-power consumption periods. To put it another way, the heat which is generated during high-power operation may be dissipated during those times when the integrated circuit is operating at less than median power.

Disclosure of the Invention

An object of an invention is to provide a temperature recognition intervention mechanism, and a method of using the same, to sense the operating temperature of an integrated circuit and to provide security against temperature-induced damaged to an integrated circuit.

Another object of the invention is to provide a mechanism and method which will detect the rate of change of temperature of an integrated circuit and adjust the rate of operation of the integrated circuit to prevent heat damage.

A further object of the invention is to provide a temperature-sensing control system which will place the chip into an "idle" status, thereby allowing builtup heat to dissipate.

The temperature-control system of the invention includes an integrated circuit and a sequence controller therefore, wherein the sequence controller provides instructions and/or data to the integrated circuit, which performs operations according to the instructions on the data. A temperature recognition intervention mechanism is provided which intervenes, via the sequence controller, with the operational rate of the integrated circuit in relation to different temperature conditions which occur in the integrated circuit, thus providing security against temperature-induced damage to the integrated circuit.

A method of the invention includes detecting a temperature-related parameter of the integrated circuit, determining the rate of change of the temperature of the integrated circuit and, if the rate of change indicates that the integrated circuit will exceed a first predetermined temperature,

providing noop instructions to the integrated circuit at a predetermined frequency, which is related to the system cycles, to allow the integrated circuit to cool and operate at a steady state temperature. If the rate of change of the temperature indicates that the integrated circuit will reach a temperature higher than a second predetermined temperature value, additional noop instructions will be provided or the integrated circuit will be shut down. A modified method of the invention adjusts the frequency at which the operations in the integrated circuit take place.

Brief Description of the Drawings

Fig. 1 is a block diagram of the temperature-sensing control system of the invention.

Fig. 2 is a graph representing power consumption and temperature over time of the integrated circuit of the invention.

Fig. 3 is a side elevation of an integrated circuit installation constructed according to the invention.

Fig. 4 is a side elevation of an integrated circuit installation constructed according to the invention, wherein a temperature sensor is integrally formed with the integrated circuit.

Fig. 5 is a schematic diagram of the integrally formed temperature sensor of Fig. 4.

Fig. 6 is a block diagram depicting the method of the invention.

Best Mode for Carrying Out the Invention

Turning initially to Fig. 1, a temperature-sensing control system constructed according to the invention is shown generally at 10. The system functions like a thermostat to achieve a steady-state operating temperature for an integrated circuit or array of integrated circuits. System 10 includes a sequence controller 12 which is operable to provide instructions and/or data to an array 14 of semi-conductor chips, such as those depicted at 16 and 18. Chips 16 and 18, collectively referred to herein as an integrated circuit, or chip, are of the single-instruction stream, multiple-data stream (SIMD) type, and are of CMOS construction. Such chips are generally designed to operate at a maximum power of 5 watts. Although specific power values are discussed

herein, it should be appreciated that such values are includes for the purpose of illustration only.

In any CMOS chip, if a part of the circuitry, such as a multiplier, is not being tasked for a particular system cycle, no power is used and no heat is generated. The unit is in a quiescent state. The only time that power is used and heat generated is during a transition or an operation. In the case of SIMD chips, all components of the chip may become active simultaneously and operate for a short period of time, thereby drawing full system power and generating a great deal of heat. The heat generated in each chip is detected by temperate sensor, or temperature sensor means, such as those depicted at 20 and 22.

Temperature sensors 20 and 22 may be integrally formed with the integrated circuit, in which case they are directly, thermally connected to the integrated circuit, or they may be attached to mounting hardware for the chip, thereby being indirectly, thermally connected to the integrated circuit. The sensors generate a temperature relevant signal which is transmitted over a connection 24 to a temperature control mechanism 26.

In the preferred embodiment, sensors 20, 22 generate an analog signal which is converted by an analog-to-digital converter 28 to a digital temperature relevant signal, which is transmitted on a connection 30.

A microprocessor controller 32 analyzes the digital temperature relevant signal and converts the signal into a temperature signal which is indicative of the rate of temperature change, T. control mechanism 26 includes a proportional integral derivation (PID) control which monitors the rate of change of the temperature of the integrated circuits which are connected to temperature control mechanism 26.

A PID applies a feedback which is proportional to the temperature error, i.e., how much hotter is T than the reference. A linear control term is used to make this determination. The error is integrated to determine if, in fact, an error is present. A derivative is calculated to determine the rate of error change. A suitable PID controller is the Intel 8022 or 8041 circuit, which includes a PID alorithm library, and which may be easily mounted on a circuit board containing ICs 16 and 18.

The PID control determines the rate of change of the integrated circuit temperature from the temperature relevant signal and determines a temperature signal therefrom. This technique of analyzing the temperature relevant signal is preferred because of the thermal inertia which is present between the integrated circuit as a whole and the temperature sensor, regardless of whether the temperature sensor is integrally formed with the chip or indirectly thermally connected thereto.

A temperature signal indicative of the rate of temperature change is transmitted from controller 32 over connection 34 to a hold control, or hold means, 38. Hold control 36 may be a discrete component, or it may be incorporated into sequence controller 12. In either configuration, hold controller 36 is associated with the sequence controller and is operable to slow the operation of the integrated circuits by a first predetermined amount if the temperature signal reaching the hold control exceeds a first predetermined value and is operable to slow the operation of the integrated circuit by a second predetermined amount or to stop operation of the integrated circuit if-and-only-if (iff) the temperature signal exceeds a second predetermined, higher value, which is less than that temperature value at which permanent damage might occur to the integrated circuits of array 14.

As used herein, the temperature sensors and the components other than the integrated circuits and sequence controller are referred to as temperature recognition intervention means, which is operably associated with the integrated circuit and constructed to intervene, via the sequence controller, with the operational rate of the integrated circuit in relation to different temperature conditions occurring in the integrated circuit, thus to promote security against temperature induced damage to the integrated circuit.

The temperature control mechanism is also referred to herein as a means associated with the temperature sensors for examining the temperature signal generated thereby for a predetermined relationship, wherein the predetermined relationship requires that the temperature signal exceed, in each instance, a first and second predetermined values prior to the hold means either slowing or stopping operation of the integrated circuits.

When the ICs are operating in boundary conditions, sufficient cooling is available and the chip is able to dissipate heat as the heat is generated as the result of chip operation. The IC operates in a stable condition where noop cycles are not required.

In the event that the hold control and sequence controller receive a temperature signal which is above the first predetermined temperature value, the sequence controller transmits a series of noop instructions over connection 38 which essentially puts the integrated circuits into an "idle" mode, where the integrated circuits cease performing any functions. This particular form of the invention does not affect the cycle clock of the overall system. It merely sends "do nothing" (noop) instructions to the integrated circuits until such time as a temperature signal is received which indicates that the integrated circuits are projected to reach an acceptable operating temperature, or after a predetermined number of system cycles have passed. At such time, normal instruction commands are transmitted over connection 38 and the integrated circuits resume normal operation.

A noop instruction, command or signal typically has a duration of 40nsec. As the operating temperature begins to increase, noop commands will be generated at a rate of 1 noop command/μsec, which is a ration of approximately 1:20, or 1 noop/500 cycles. It should be appreciated that the rate of noop commands will vary as the PID controller attempts to achieve a steady-state operating temperature which has minimal temperature oscillations during the operation of the IC.

In the event that a rapid temperature rise is detected in the integrated circuits, such that the rate of temperature change indicates that the integrated circuits will reach a temperature above their maximum safe operating temperature, sequence controller 12 will shut down the system containing the integrated circuits to prevent permanent damage to the array, or will transmit a larger number of noop commands to allow the IC to cool. The system may be restarted by an externally generated command once an appropriate temperature has been reached. Such a situation is not expected to occur under normal operating conditions, however, in the event that the programming for the system contains a "bug" which puts the integrated circuits

into continuous, maximum power operation, it is foreseeable that the operating temperature may exceed the safe maximum.

Turning now to Fig. 2, a graph depicting power consumption of the integrated circuits of array 14 verses time is shown. As previously noted, integrated circuits, such as 16 and 18, operate under the command of sequence controller 12 in what may be thought of as a "bursty" fashion, i.e., the integrated circuits tend to operate with no or minimal activity for a period of time and then operate at maximum, or close to maximum capacity for a period of time. This activity is depicted by trace 40. Assuming that the maximum power draw of an integrated circuit of the invention is 5 watts, and that the circuit is constructed for a nominal 2 watt power consumption, as indicated by line 42, it may be seen that the integrated circuits tend to operate above and below their design level over time. Because of thermal inertia, the actual temperature of the integrated circuit lags behind the power consumption, as indicated by line 44. Under normal operating conditions, the regions of trace 40 which are above the 2 watt line 42 may be thought of as filling in the valleys, thus "averaging" the temperature of the integrated circuit. It should be noted that the activity depicted by lines 40 and 44 do not cause the temperature to rise to the level of T_1, which represents the first predetermined value, and which, in the preferred embodiment, is between about 90°C and 100°C, nor the level of T_2 which represents the second predetermined value, and which, in the preferred embodiment, has a value greater than 150°C.

In the event of continued activity of a particular duty cycle, such as indicated by dashed line 46, the temperature may exceed T_1, as represented by dashed temperature line 44a, and which occurs at point 48. Upon receipt of a temperature signal indicating that a ΔT which will cause a chip to exceed T_1, sequence controller 12 begins sending noop signals to the integrated circuits, thereby reducing power consumption and, after the temperature falls below T_1, as indicated at point 50, or, after a predetermined number of system cycles has occurred, the sequence controller begins to send normal instructions to the integrated circuits.

Another way of describing the activity of the integrated circuits in array 14 is that they initially sit idle. Then they receive a great deal of data from sequence controller 12, perform their task and then are idle. Because

cooling hardware is expensive and occupies a great deal of space, and because the integrated circuits in array 14 are very expensive, it is desirable to protect the circuits from heat damage, particularly that type of heat damage which is generated by the integrated circuit itself. Hold control 36 may also be constructed to slow the system clock for the IC array.

Turning now to Fig. 3, a mounting arrangement for an integrated circuit and temperature sensor is depicted. The mounting includes a circuit board 52 and a circuit holder 54, which have an integrated circuit, such as integrated circuit 16 sandwiched there between. A heat sink 56 is attached to circuit holder 54 and includes fins 58 to dissipate heat. A temperature sensor 60 is mounted on heat sink 56 and provides a temperature relevant signal to the temperature control mechanism. A suitable temperature sensor for this arrangement is that manufactured by NSC Corporation under the designation LM35.

Turning to Fig. 4, an arrangement with a temperature sensor 62 integrally formed with integrated circuit 16 is depicted. Fig. 5 depicts sensor 62 as including a temperature sensitive induction mechanism 64 which is connected to the voltage supply 66 of the circuit. Sensor 62 includes a diode 68 between induction mechanism 64 and ground 70. An amplifier 72 is provided to boost the temperature relevant signal generated by sensor 62. For low duty cycle operations, such as speech recognition, a heat sink may not be required to maintain the desired IC operating temperature.

Fig. 6 depicts the steps in carrying out the method of the invention. A sensor transmits a temperature related signal, block 74, to temperature control mechanism 26. Temperature control mechanism 26, and specifically the PID controller, determines the ΔT from successive temperature related signals, block 76. The ΔT value is transmitted to hold control 36.

Hold control 36 determines if ΔT is indicative of a temperature of the integrated circuit which is greater than T_1, block 78. If not, the operation of the system continues, block 80. If ΔT indicates that the temperature of the integrated circuit 14 is greater than T_1, sequence controller 12 sends a series of noop signals for a predetermined number (N) system cycles, block 82. N cycles should be sufficient to allow cooling of integrated circuit 14 to a temperature below T_1.

If hold control 36 detects a ΔT which will raise the temperature of integrated circuit 14 above T_2, block 84, the system is shut down, block 86. If the ΔT is indicative of a temperature below T_1 and T_2, the system continues normally, block 88.

For ΔTs which project a T between T_1 and T_2, the frequency of the noop commands will increase to achieve a steady state temperature. System 10 acts like a linear control system at projected temperatures below T_2, above which it functions in a non-linear control system.

The effect of sending noop signals to integrated circuit 14 is to "slow" the total system computation down by inserting idle clock cycles, thereby allowing more time for the generated heat to dissipate from the integrated circuit, using thermal inertia to "average" the temperature of the chip to an acceptable level. In most instances, the slow down caused by temperature control will probably go unnoticed by the system operator. The only significant event will occur if there is an endless loop which causes integrated circuit 14 to operate at maximum power for an extended period of time.

The noop signal which is transmitted from sequence controller 12 is appropriate when integrated circuits in array 14 contain static storage components as is normal in CMOS design. In the case of dynamic storage, such as where information is placed in a capacitor like device, the "information" will tend to dissipate and must be periodically refreshed. A "refresh" command must be asserted periodically while such a system is waiting for its next active period. The refresh command, for dynamic storage is equivalent to the noop command for static storage and may be used in the event that the chips in array 14 contain dynamic memory.

Another benefit of equipping any IC or IC array with control system 10 is that the IC or array will operate at a steady temperature which will prolong the life of the IC or array components.

It should be appreciated that array 14 may contain any number of integrated circuits, additionally, the "array" may contain a single integrated circuit. The temperature sensors that are associated with each integrated circuit feed into a common connection 24. Microprocessor controller 32 may contain sequencing information to sort out the signals from individual integrated circuits. Because sequence controller 12 transmits a single

instruction to all of the integrated circuits in array 14, an unacceptable temperature rise on any integrated circuit will necessarily result in all of the integrated circuits in the array receiving noop signals.

Industrial Application

The temperature-sensing control system is well suited for use on CMOS integrated circuits, and particularly for CMOS SIMD/Neural Network integrated circuits whose temperature is dependant on the amount of activity which has taken place in circuitry contained in the chip, or for any integrated circuit that operates in a limited power environment.

WHAT I CLAIM IS:

1. A temperature-sensing control system for use on an integrated circuit comprising:

an integrated circuit (14) having a sequence controller (12) operatively connected thereto, said sequence controller (12) providing instructions and/or data to said integrated circuit (14) which performs operations according to said instructions on said data;

temperature sensor means (20) thermally connected to the integrated circuit (14) and means associated with said temperature sensor means therewith for creating a temperature signal; and

hold means (36) associated with said sequence controller (12) for slowing operation of said integrated circuit (14) by a predetermined amount if said temperature signal has a predetermined relationship to a first predetermined value and for slowing operation of said integrated circuit (14) by a greater predetermined amount if said temperature signal has a predetermined relationship to a second predetermined value, which second predetermined value is higher than said first predetermined value.

2. The temperature-sensing control system of claim 1 wherein said greater predetermined amount is sufficient to stop operation of said integrated circuit (14).

3. The temperature-sensing control system of claim 1 wherein said means associated includes a temperature control mechanism (26) for examining said temperature signal for said predetermined relationship.

4. The temperature-sensing control system of claim 3 wherein said predetermined relationship requires that the temperature signal exceed, in each instance, said first and second predetermined values.

5. A temperature-sensing control system for use on an integrated circuit comprising:

an array of integrated circuits (14) having a single sequence controller (12) operatively connected thereto, said sequence controller (12) providing instructions and/or data to said integrated circuit (14) which performs operations according to said instructions on said data;

temperature sensor means (20) thermally connected to the integrated circuit (14) for generating a temperature relevant signal;

a temperature control mechanism (26) for converting said temperature relevant signal into a temperature signal; and

hold means associated with said sequence controller (12) for slowing operation of said integrated circuit (14) if said temperature signal exceeds a first predetermined value and for further slowing operation of said integrated circuit (14) iff said temperature signal exceeds a second predetermined value, which second predetermined value is higher than said first predetermined value.

6. The temperature-sensing control system of claim 5 wherein said greater predetermined amount is sufficient to stop operation of said integrated circuit (14).

7. The temperature-sensing control system of claim 5 wherein said temperature control mechanism (26) includes a proportional integral derivation control which determined the rate of change of said integrated circuit (14) temperature from said temperature relevant signal and for determining said temperature signal therefrom.

8. The temperature-sensing control system of claim 5 wherein said hold means (36) includes a mechanism for sending noop instructions to said integrated circuit (14) for a predetermined number of system cycles at a predetermined frequency upon receipt of a first predetermined temperature value.

9. The temperature-sensing control system of claim 5 wherein said hold means (36) includes a mechanism for slowing the system clock of said integrated circuit (14).

10. The temperature-sensing control system of claim 5 wherein said temperature sensor (20) is integrally formed with said integrated circuit (14).

11. The temperature-sensing control system of claim 10 wherein said temperature sensor (20) includes a temperature-sensitive induction mechanism (64).

12. The temperature-sensing control system of claim 5 wherein said temperature sensor (20, 60) includes a heat sink (56) thermally connected to said integrated circuit (14) and said temperature sensor (20, 60) is mounted on said heat sink (56).

13. The temperature-sensing control system of claim 5 wherein the temperature of said integrated circuit (14) is dependant on and proportional to the amount and type of computations which said integrated circuit (14) carries out.

14. A temperature-sensing control system for use on an integrated circuit comprising:

an integrated circuit (14) having a sequence controller (12) operatively connected thereto, said sequence controller (12) providing instructions and/or data to said integrated circuit (14) which performs operations according to said instructions on said data; and

temperature recognition intervention means operatively associated with said integrated circuit (14) and constructed to intervene, via said sequence controller (12), with the operational rate of said integrated circuit (14) in relation to different temperature conditions occurring in the integrated circuit

(14), thus to promote security against temperature-induced damage to the latter.

15. The temperature-sensing control system of claim 14 wherein said temperature-recognition intervention means includes a temperature sensor (20) thermally connected to said integrated circuit (14) and means associated therewith for creating a temperature relevant signal.

16. The temperature-sensing control system of claim 15 wherein said temperature-recognition intervention means further includes a temperature control mechanism (26) for converting said temperature relevant signal into a temperature signal and hold means associated with said sequence controller (12) for slowing operation of said integrated circuit (14) if said temperature signal exceeds a first predetermined value and for further slowing operation of said integrated circuit (14) iff said temperature signal exceeds a second predetermined value, which second predetermined value is higher than said first predetermined value.

17. The temperature-sensing control system of claim 16 wherein said greater predetermined amount is sufficient to stop operation of said integrated circuit (14).

18. The temperature-sensing control system of claim 16 wherein said temperature control mechanism (26) includes a proportional integral derivation control which determines the rate of change of said integrated circuit (14) temperature from said temperature relevant signal and for determining said temperature signal therefrom.

19. The temperature-sensing control system of claim 16 wherein said hold means (36) includes a mechanism for sending noop instructions to said integrated circuit (14) for a predetermined number of system cycles at a predetermined frequency upon receipt of a first predetermined temperature value.

20. The temperature-sensing control system of claim 16 wherein said hold means (36) includes a mechanism for slowing the system clock of said integrated circuit (14).

21. The temperature-sensing control system of claim 16 wherein said temperature sensor (20, 62) is integrally formed with said integrated circuit (14).

22. The temperature-sensing control system of claim 21 wherein said temperature sensor (20, 62) includes a temperature-sensitive induction mechanism.

23. The temperature-sensing control system of claim 16 wherein said temperature sensor (20, 60) includes a heat sink (56) thermally connected to said integrated circuit (14) and said temperature sensor (20, 60) is mounted on said heat sink (56).

24. The temperature-sensing control system of claim 16 wherein the temperature of said integrated circuit (14) is dependant on and proportional to the amount and type of computations which said integrated circuit (14) carries out.

25. A method of controlling the temperature of an integrated circuit comprising:

providing an integrated circuit (14) which operates under the control of a sequence controller (12);

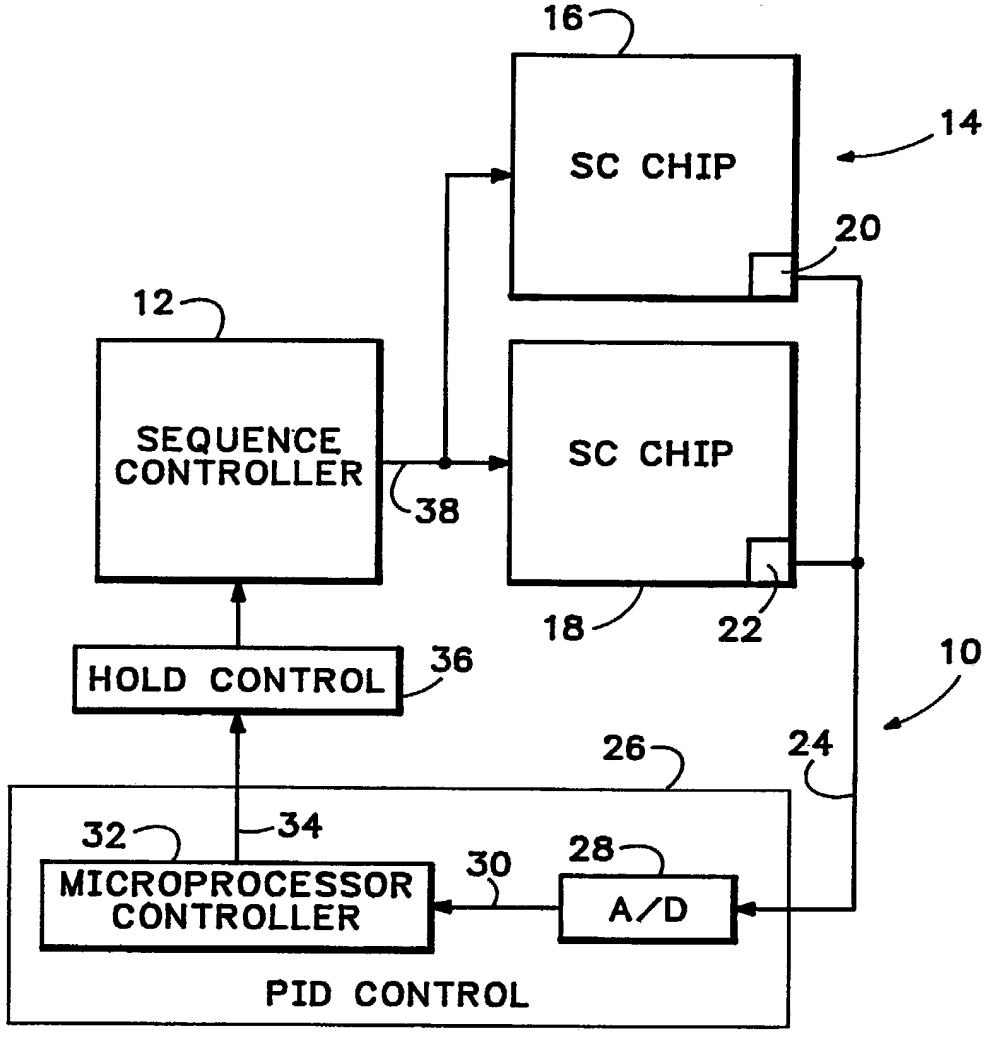
providing a temperature sensor (20) in thermal connection with the integrated circuit (14);

generating (74) a temperature-relevant signal from the temperature sensor (20);

determining the rate of change (76) of the temperature (ΔT) of the integrated circuit (14);

sending the ΔT to a hold control (36);

generating, from the hold control, a noop signal (82) for a predetermined number of system cycles if the ΔT indicates that the temperature of the integrated circuit (14) will exceed a first predetermined temperature value, and, generating a stop operations signal (86) from the hold control iff the ΔT indicates that the temperature of the integrated circuit (14) will exceed a second, higher, predetermined value.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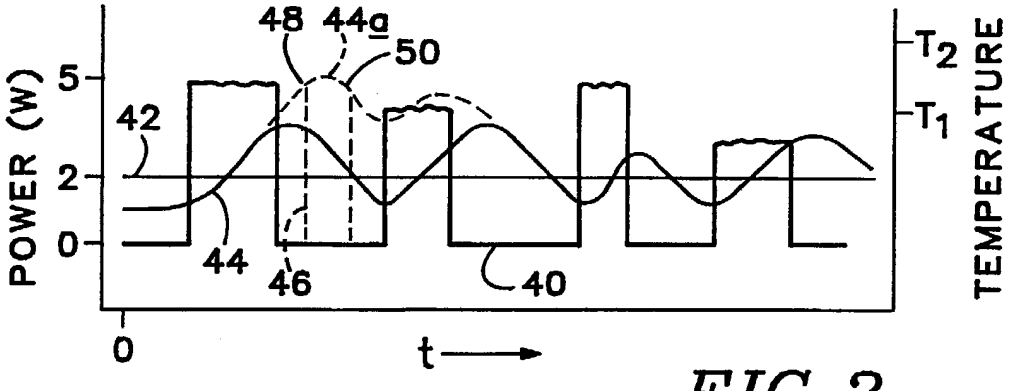
SC CHIP
14
20
12
SEQUENCE CONTROLLER
38
SC CHIP
18
22
10
HOLD CONTROL
36
26
24
32
34
MICROPROCESSOR CONTROLLER
30
28
A/D
PID CONTROL

FIG. 1


48
44a
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T_1
POWER (W)
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42
44
46
40
TEMPERATURE
0
t

FIG. 2

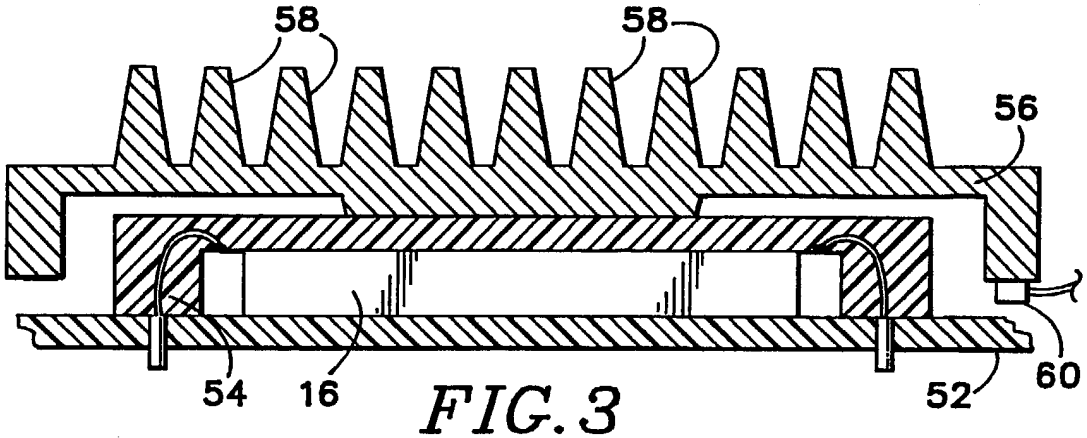


FIG. 3

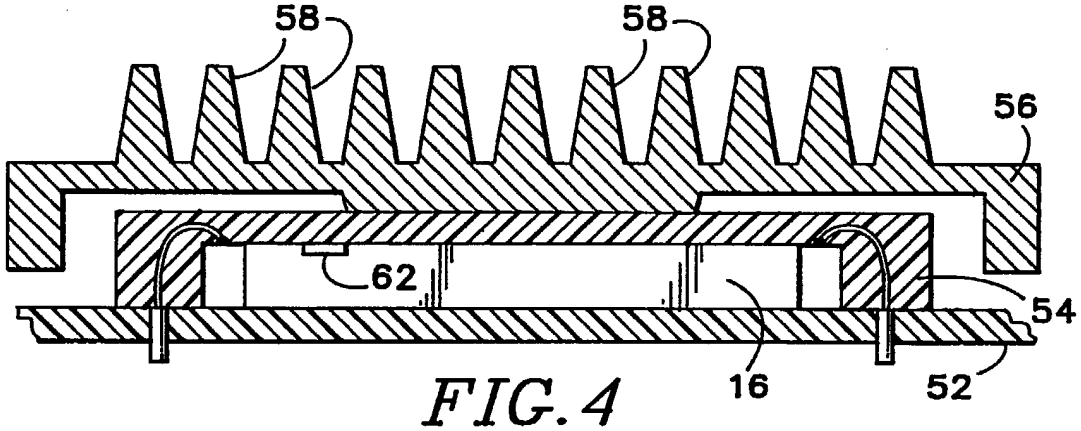


FIG. 4

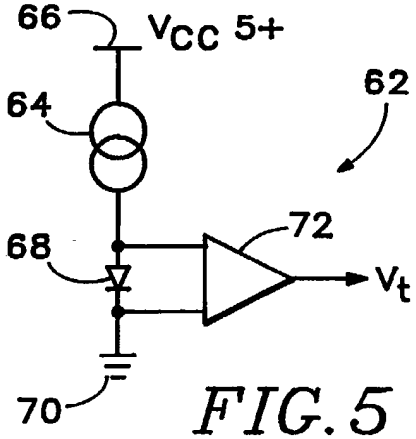
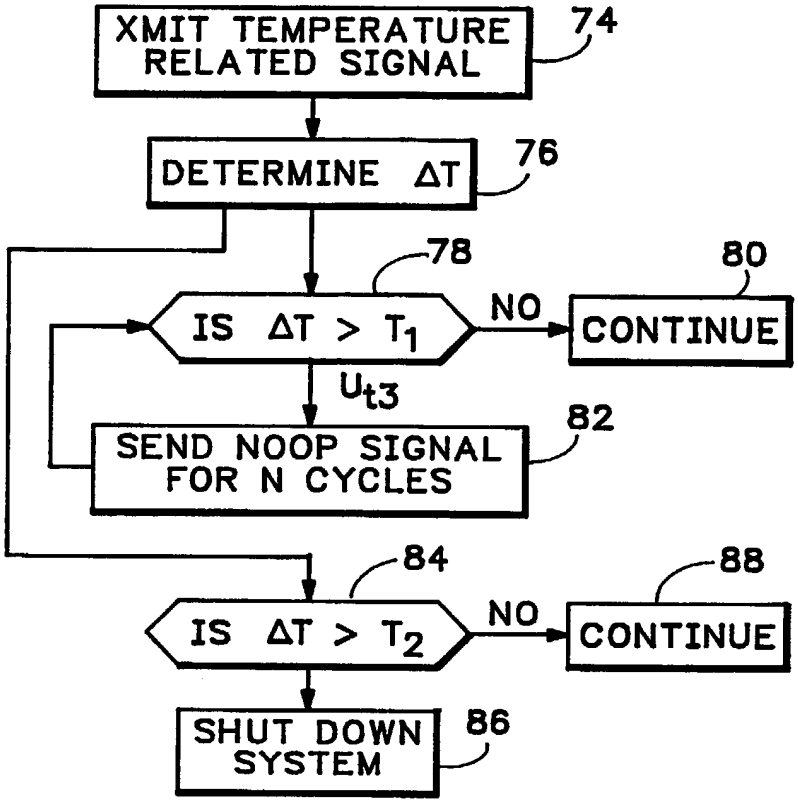


FIG. 5


XMIT TEMPERATURE RELATED SIGNAL
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DETERMINE ΔT
76
78
80
IS ΔT > T1
NO
CONTINUE
Ut3
SEND NOOP SIGNAL FOR N CYCLES
82
84
88
IS ΔT > T2
NO
CONTINUE
SHUT DOWN SYSTEM
86

FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/06878

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): H03K 17/08
U.S.Cl.: 361/103; 384/557; 371/4

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S	361/1,103; 371/4,14; 364/557 374/168,173

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4,924,112 (ANDERSON ET AL.) 08 May 1990 See abstract	1-25
A	US, A, 4,307,463 (SIBLEY) 22 December 1981 See entire document	1-25
A	US, A, 4,868,817 (SHIGIHARA) 19 September 1989 See entire document	1-25

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
10 April 1991	29 APR 1991
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	for Todd E. Deboer

Form PCT/ISA/210 (second sheet) (May 1986)